Ref #	Hits	Search Query	DBs	Default Operat or	Plura Is	Time Stamp
Li	1	JUNGHAK NEAR1 KIM	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	AND	ON	2006/11/30 11:10
L2	1343	"8b/10b"	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	AND	ON	2006/11/30 11:12
L3	12	"8b/10b" validity	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2006/11/30 11:17
L4	1	"8b/10b" validity "6b/5b"	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2006/11/30 11:18

L5	1	"8b/10b" "6b/5b"	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2006/11/30 11:18
L6	51	"8b/10b" valid\$5 disparity	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2006/11/30 11:19
L7	2	"8b/10b" valid\$5 disparity nibble	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2006/11/30 11:21
L8	2	"8b/10b" valid\$5 disparity nibble ("6" ADJ1 bit)	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2006/11/30 12:26

11/30/06 2:34:04 PM

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L9	1	"8b/10b" valid\$5 disparity nibble ("6" ADJ1 bit) AND significant	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2006/11/30 11:25
L10	2	"8b/10b" valid\$5 disparity nibble ("6" ADJ1 bit) AND least	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2006/11/30 12:34
L11	. 1	"8b/10b" valid\$5 disparity nibble ("6" ADJ1 bit) AND most	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2006/11/30 11:26
L12	1	"8b/10b" disparity nibble ("6" ADJ1 bit) AND most	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2006/11/30 11:26

L13	6	"8b/10b" disparity ("6" ADJ1 bit) AND most	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2006/11/30 11:27
L14	0	"8b/10b" disparity ("6" ADJ1 bit) AND (most significant of msb)	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2006/11/30 11:28
L15	0	"8b/10b" disparity ("6" ADJ1 bit) AND (most ADJ1 significant of msb)	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2006/11/30 11:28
L16	1	"8b/10b" disparity ("6" ADJ1 bit) AND (most ADJ1 significant or msb)	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2006/11/30 12:27

L17	4	(Tae Whan NEAR1 Yoo) or (Hyeong Ho NEAR1 Lee)	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	WITH	ON	2006/11/30 12:16
L18	102	(Tae Whan Yoo) or (Hyeong Ho Lee)	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	WITH	ON	2006/11/30 12:16
L19	. 4	((Tae Whan Yoo) or (Hyeong Ho Lee)) and disparity	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	WITH	ON	2006/11/30 12:17
L20	1	((Tae Whan Yoo) or (Hyeong Ho Lee)) and disparity validity SAME "8b/10b"	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	WITH	ON	2006/11/30 12:18

L21	1	((Tae Whan Yoo) or (Hyeong Ho Lee)) and validity SAME "8b/10b"	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	WITH	ON	2006/11/30 12:19
L22	6	((Tae Whan Yoo) or (Hyeong Ho Lee)) and "8b/10b"	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	WITH	ON	2006/11/30 12:19
L23	0	"8b/10b" "4b/3b"validity disparity nibble	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	AND	ON C	2006/11/30 12:26
L24	1	"8b/10b" "4b/3b" validity disparity nibble	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	AND	ON	2006/11/30 12:26

L25	1	"8b/10b" disparity (most ADJ1 significant or msb)	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2006/11/30 12:28
L26	21	"8b/10b" disparity most	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2006/11/30 12:28
L27	1	"8b/10b" disparity most significant	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2006/11/30 12:28
L28	67	"8b/10b" WITH valid\$5	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2006/11/30 12:36

L29	1	"8b/10b" WITH valid\$5 WITH "6"	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2006/11/30 12:36
L30	4	"8b/10b" valid\$5 "6" ADJ1 bit	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD	SAME	ON	2006/11/30 12:40
			B.	-		
L31	1	"8b/10b" valid\$5 "6" ADJ1 bit (most or msb)	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2006/11/30 12:39
L32	4	"8b/10b" valid\$5 "6" ADJ1 bit disparity	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2006/11/30 12:49

L33	1	"8b/10b" valid\$5 "6" ADJ1 bit disparity rule	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2006/11/30 12:50
L34	3	"8b/10b" valid\$5 disparity rule	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2006/11/30 12:51
L35	1	"8b/10b" valid\$5 disparity rule most	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2006/11/30 12:51
L36	2	"8b/10b" valid\$5 disparity rule least	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2006/11/30 12:52

L37	1	"8b/10b" valid\$5 disparity most least	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2006/11/30 12:55
L38	27	"8b/10b".ti.	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2006/11/30 13:08
L39	2	"8b/10b".ti. and line ADJ1 code	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2006/11/30 13:07
L40	9	"8b/10b".ti. line	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	AND	ON	2006/11/30 13:12

11/30/06 2:34:04 PM Page 10

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L41	2	"8b/10b".ti. and code rule violat\$5	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	WITH	ON	2006/11/30 13:17
L42	2	"8b/10b".ti. and code rule (valid\$4 OR violat\$5)	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	WITH	ON	2006/11/30 13:19
L43	0	8bit 10bit code rule (valid\$4 OR violat\$5)	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	WITH	ON	2006/11/30 13:19
L44	0	8bit 10bit (valid\$4 OR violat\$5)	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	WITH	ON	2006/11/30 13:19

L45	81	("8" ADJ1 bit) ("10" ADJ1 bit) (valid\$4 OR violat\$5)	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	WITH	ON	2006/11/30 13:21
L46	8	("8" ADJ1 bit) ("10" ADJ1 bit) disparity (valid\$4 OR violat\$5)	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	WITH	ON	2006/11/30 13:45
L47	6	("4486739" "4975916" "5 229769").PN.	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	AND	ON	2006/11/30 13:29
L48	0	2001-0064238	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	AND	ON	2006/11/30 13:37

11/30/06 2:34:04 PM

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L49	38	"0064238"	US-PGPU B; USPAT; USOCR; EPO;	AND	ON	2006/11/30 13:39
			JPO; DERWEN T; IBM_TD B			
L50	0	LEE NEAR1 HYUNG-SEOP	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T;	AND	ON.	2006/11/30 13:40
			IBM_TD_ B		र मध्य	
L51	0	LEE NEAR1 HYUNG NEAR SEOP	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T;	AND	ON	2006/11/30 13:40
			IBM_TD B	7.1.	<i>?</i> "	skare, e e
L52	0	LEE ADJ1 HYUNG ADJ1 SEOP	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	AND	ON	2006/11/30 13:56

11/30/06 2:34:04 PM

L53	43	"0062388"	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	AND	ON	2006/11/30 13:42
L54	6	gigabit "8b/10"	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD	SAME	ON	2006/11/30 13:45
L55	0	(most ADJ1 significant or msb or upper) "8b/10"	B US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	WITH	ON	2006/11/30 13:46
L56	0	(most ADJ1 significant or msb or upper) "8b/10"	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2006/11/30 13:46

						
L57	2	(significant or msb or upper) "8b/10"	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2006/11/30 13:47
L58	38	"0064238"	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	SAME	ON	2006/11/30 13:48
L59	0	"0064238" gigabit	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	AND	ON	2006/11/30 13:49
L60	0	"2001-0064238" gigabit	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	AND	ON	2006/11/30 13:49
L61	776	(341/55,58,95).CCLS.	USPAT	OR	OFF	2006/11/30 13:57

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L62	1343	8b/10b	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	AND	ON	2006/11/30 13:58
L63	1343	"8b/10b"	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	AND	ON	2006/11/30 13:58
L64	51	"8b/10b" and l61	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	AND	ON	2006/11/30 13:58
L65	5	"8b/10b" valid\$4 and l61	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	WITH	ON	2006/11/30 14:02

11/30/06 2:34:04 PM

L66	5	"8b/10b" (valid\$4 or violAT\$4) and l61	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	WITH	ON	2006/11/30 14:03
L67	82	"8b/10b" (valid\$4 or violAT\$4)	US-PGPU B; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	WITH	ON	2006/11/30 14:03



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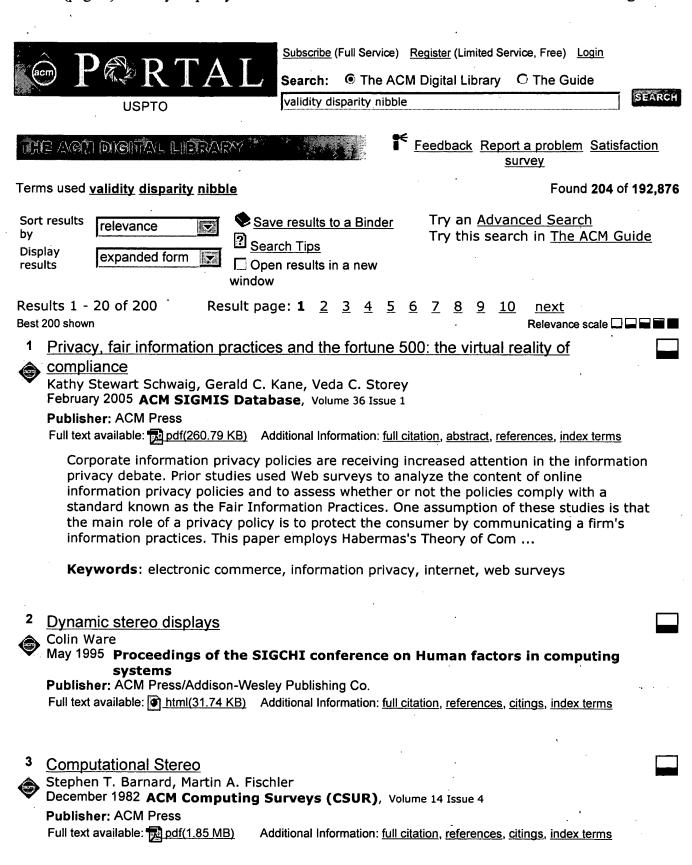
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January 1984 ACM SIGARCH Computer Architecture News, Proceedings of the 11th

annual international symposium on Computer architecture ISCA '84,

Experimental evaluation of on-chip microprocessor cache memories

Mark D. Hill, Alan Jay Smith

Volume 12 Issue 3

Publisher: ACM Press Additional Information: full citation, abstract, references, citings, index Full text available: pdf(943.62 KB) terms Advances in integrated circuit density are permitting the implementation on a single chip of functions and performance enhancements beyond those of a basic processors. One performance enhancement of proven value is a cache memory; placing a cache on the processor chip can reduce both mean memory access time and bus traffic. In this paper we use trace driven simulation to study design tradeoffs for small (on-chip) caches. Miss - ratio and traffic ratio (bus traffic) are the metrics for cache p ... A hardware-based performance monitor for the Intel iPSC/2 hypercube Allen D. Malony, Daniel A. Reed June 1990 ACM SIGARCH Computer Architecture News, Proceedings of the 4th international conference on Supercomputing ICS '90, Volume 18 Issue 3b Publisher: ACM Press Additional Information: full citation, abstract, references, citings, index Full text available: pdf(1.50 MB) terms The complexity of parallel computer systems makes a priori performance prediction difficult and experimental performance analysis crucial. A complete characterization of software and hardware dynamics, needed to understand the performance of highperformance parallel systems, requires execution time performance instrumentation. Although software recording of performance data suffices for low frequency events, capture of detailed, high-frequency performance data ultimately r ... Service quality in the management of simulation projects Stewart Robinson, Michael Pidd December 1995 Proceedings of the 27th conference on Winter simulation **Publisher: ACM Press** Full text available: pdf(679.79 KB) Additional Information: full citation, references, index terms Computer system design using a hierarchical approach to performance evaluation B. Kumar, E. S. Davidson September 1980 Communications of the ACM, Volume 23 Issue 9 Publisher: ACM Press Full text available: pdf(1.07 MB) Additional Information: full citation, abstract, references, citings The concept of a hierarchy of performance models is introduced. It is argued that such a hierarchy should consist of models spanning a wide range of accuracy and cost in order to be a cost-effective tool in the design of computer systems. Judicious use of the hierarchy can satisfy the conflicting needs of high accuracy and low cost of performance evaluation. A system design procedure that uses the hierarchy is developed. The concepts developed are illustrated by applying them to ... Keywords: hierarchical modeling, high speed computer systems, optimization algorithms, performance evaluation, system design Plenoptic modeling: an image-based rendering system Leonard McMillan, Gary Bishop September 1995 Proceedings of the 22nd annual conference on Computer graphics

and interactive techniques

Publisher: ACM Press

Full text available: pdf(347.37 KB) Additional Information: full citation, references, citings, index terms ps(3.98 MB)

9	The partial-occlusion effect: utilizing semitransparency in 3D human-computer interaction Shumin Zhai, William Buxton, Paul Milgram September 1996 ACM Transactions on Computer-Human Interaction (TOCHI), Volume 3 Issue 3 Publisher: ACM Press	
	Full text available: pdf(6.54 MB) Additional Information: full citation, abstract, references, citings, index terms	
	This study investigates human performance when using semitransparent tools in interactive 3D computer graphics environments. The article briefly reviews techniques for presenting depth information and examples of applying semitransparency in computer interface design. We hypothesize that when the user moves a semitransparent surface in a 3D environment, the "partial-occlusion" effect introduced through semitransparency acts as an effective cue in target localization—an ess	
	Keywords : 3D interfaces, depth perception, partial occlusion, semitransparency, stereopsis	
10	Program verification: the very idea	
*	James, H. Fetzer August 1988 Communications of the ACM, Volume 31 Issue 9	
	Publisher: ACM Press	
	Full text available: pdf(2.09 MB) Additional Information: full citation, abstract, references, citings, index terms, review.	•
	The notion of program verification appears to trade upon an equivocation. Algorithms, as logical structures, are appropriate subjects for deductive verification. Programs, as causal models of those structures, are not. The success of program verification as a generally applicable and completely reliable method for guaranteeing program performance is not even a theoretical possibility.	
11 (*)	An empirical study of the relationships between IT infrastructure flexibility, mass customization, and business performance Sock H. Chung, Terry Anthony Byrd, Bruce R. Lewis, F. Nelson Ford August 2005 ACM SIGMIS Database, Volume 36 Issue 3	
	Publisher: ACM Press	
	Full text available: pdf(339.00 KB) Additional Information: full citation, abstract, references, index terms	
	Information technology (IT) infrastructure deserves serious attention from both the practitioner and academic communities, especially concerning the factors for IT infrastructure flexibility. The issue of flexibility is viewed as a critical aspect of IT infrastructure, because organizations are faced with an ever-increasing rate of change in their business environments. One effort most business sectors have made to prepare for this change is the trend toward mass customization. Recently, many or	

Keywords: IT compatibility, IT connectivity, IT infrastructure flexibility, IT modularity, IT personnel skills, business performance, mass customization

Modeling methodology a: Optimization and response surfaces: an optimization-based

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	multi-resolution simulation methodology Darren T. Drewry, Paul F. Reynolds, William R. Emanuel December 2002 Proceedings of the 34th conference on Winter simulation: exploring new frontiers Publisher: Winter Simulation Conference	
	Full text available: pdf(249.88 KB) Additional Information: full citation, abstract, references	
	The need for new approaches to the consistent simulation of related phenomena at multiple levels of resolution is great. While many fields of application would benefit from a complete and approachable solution to this problem, such solutions have proven extremely difficult. We present a multi-resolution simulation methodology which uses numerical optimization as a tool for maintaining external consistency between models of the same phenomena operating at different levels of temporal and/or sp	
13	Nonblocking copy networks in multi-channel switching Paul S. Min, Manjunath V. Hegde, Hossein Saidi, Alex Chandra December 1995 IEEE/ACM Transactions on Networking (TON), Volume 3 Issue 6 Publisher: IEEE Press	
	Full text available: pdf(1.31 MB) Additional Information: full citation, references, index terms	
	Research contributions: The impact of culture and gender on web sites: an empirical study Steven John Simon	
	December 2000 ACM SIGMIS Database, Volume 32 Issue 1 Publisher: ACM Press	•
	Full text available: pdf(1.88 MB) Additional Information: full citation, abstract, references, citings, index terms	
	The growth of electronic commerce, in particular business-to-consumer, has been explosive during the last few years. Until recently, the Web community has been a male dominated western-oriented society, with the design of Web sites reflecting that homogenous audience. Using an adapted version of Hofstede's dimensions as a means of differentiation, this study explores the perception and satisfaction levels of one hundred and sixty subjects on four web sites. Analysis indicates that perception and	
	Keywords : Hofstede model, e-commerce, gender differences (satisfaction & perception), web site design	
15	Similarity in harder cases: sentencing for fraud Ruth Murbach, Éva Nonn	
~	August 1993 Proceedings of the 4th international conference on Artificial intelligence and law Publisher: ACM Press	
	Full text available: pdf(943.49 KB) Additional Information: full citation, abstract, references, citings, index terms	
	We focus on one of the central concepts of case-based reasoning: similarity. In the field of sentencing, where the really decided cases are often on the harder side, similarity is multidimensional and depends less on formal rules than on various legitimate principles, objectives and factors which relate to the offender, the victim, the act and its social context. The paper presents our data base of empirically analysed cases of fraud and discusses two of the different phases completed to re	

16 Cache performance of operating system and multiprogramming workloads

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•	Anant Agarwal, John Hennessy, Mark Horowitz November 1988 ACM Transactions on Computer Systems (TOCS) , Volume 6 Issue 4	
	Publisher: ACM Press	
	Full text available: pdf(3.16 MB) Additional Information: full citation, abstract, references, citings, index terms, review	
	Large caches are necessary in current high-performance computer systems to provide the required high memory bandwidth. Because a small decrease in cache performance can result in significant system performance degradation, accurately characterizing the performance of large caches is important. Although measurements on actual systems have shown that operating systems and multiprogramming can affect cache performance, previous studies have not focused on these effects. We have developed a pro	
17	Integrating active percentian with an autonomous relativestime	
	Integrating active perception with an autonomous robot architecture Glenn Wasson, David Kortenkamp, Eric Huber	Щ
	May 1998 Proceedings of the second international conference on Autonomous	
	agents	
	Publisher: ACM Press	
	Full text available: pdf(984.62 KB) Additional Information: full citation, references, citings, index terms	
18	Operational characteristics of a harware-based pattern matcher	
\$	Roger L. Haskin, Lee A. Hollaar March 1983 ACM Transactions on Database Systems (TODS) , Volume 8 Issue 1	
	Publisher: ACM Press	
	Full text available: pdf(1.84 MB) Additional Information: full citation, abstract, references, citings, index terms	
	The design and operation of a new class of hardware-based pattern matchers, such as would be used in a backended database processor in a full-text or other retrieval system, is presented. This recognizer is based on a unique implementation technique for finite state automata consisting of partitioning the state table among a number of simple digital machines. It avoids the problems generally associated with implementing finite state machines, such as large state table memories, complex cont	
	Keywords : backend processors, computer system architecture, finite state automata, full text retrieval systems, text searching	٠
19	Possible for chicate in VD displayed for and forms and	
•	Reaching for objects in VR displays: lag and frame rate Colin Ware, Ravin Balakrishnan December 1994 ACM Transactions on Computer-Human Interaction (TOCHI), Volume 1	
	Issue 4 Publisher: ACM Press	
	Additional Information full pitation of paragraphs	
	Full text available: pdf(1.54 MB) Additional information: null citation, abstract, references, citings, index terms, review	
	This article reports the results from three experimental studies of reaching behavior in a head-coupled stereo display system with a hand-tracking subsystem for object selection. It is found that lag in the head-tracking system is relatively unimportant in predicting performance, whereas lag in the hand-tracking system is critical. The effect of hand lag can be modeled by means of a variation on Fitts' Law with the measured system lag introduced as a multiplicative variable to the Fitts' La	
	Keywords: Fitts' Law, Haptics, virtual reality	

20	Research contributions:	Testing an extended model of IT a	acceptance in the Chinese

<u>cultural context</u>

En Mao, Prashant Palvia

September 2006 ACM SIGMIS Database, Volume 37 Issue 2-3

Publisher: ACM Press

Full text available: pdf(298.95 KB) Additional Information: full citation, abstract, references, index terms

Research on technology acceptance and diffusion is critical, providing insights into how organizations can manage the adoption and use of information technology. With globalization, it is important to understand IT adoption in other cultures. The primary purpose of this study is to enrich the understanding of IT acceptance by extending a U.S.based research model to a different culture, namely China. We conducted a crosssectional survey of e-mail users in 30 Chinese organizations. Structural eq ...

Keywords: culture and IT management, management of information systems, technology acceptance

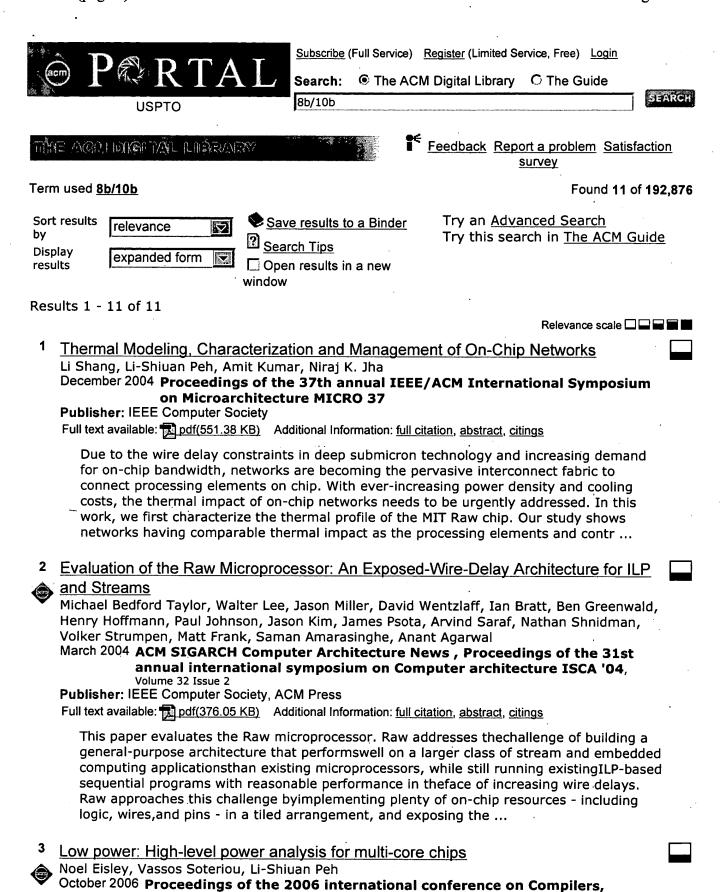
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Full text available: pdf(721.86 KB) Additional Information: full citation, abstract, references, index terms

architecture and synthesis for embedded systems CASES '06

Technology trends have led to the advent of multi-core chips in the form of both generalpurpose chip multiprocessors (CMPs)and embedded multi-processor systems-on-a-chip (MPSoCs), with on-chip networks increasingly becoming the defacto communication fabric between cores as the demand for on-chip bandwidth scales up. These multi-core chips are composed of two key subcomponents: processor cores and a network fabric. Rapid, earlystage power estimation of these multi-core chips is crucial in assis ...

Keywords: chip multiprocessor (CMP), multi-core, power analysis, simulation, systemon-a-chip (SoC)

4	Promises and reality: Server I/O networks past, present, and future Renato John Recio August 2003 Proceedings of the ACM SIGCOMM workshop on Network-I/O convergence: experience, lessons, implications NICELI '03 Publisher: ACM Press Full text available: pdf(225.62 KB) Additional Information: full citation, abstract, references, index terms Enterprise and technical customers place a diverse set of requirements on server I/O networks. In the past, no single network type has been able to satisfy all of these	
	requirements. As a result several fabric types evolved and several interconnects emerged to satisfy a subset of the requirements. Recently several technologies have emerged that enable a single interconnect to be used as more than one fabric type. This paper will describe the requirements customers place on server I/O networks; t	
	Keywords : 10 GigE, Cluster, Cluster Networks, Gigabit Ethernet, I/O Expansion Network, IOEN, InfiniBand, LAN, PCI, PCI Express, RDMA, RNIC, SAN, Socket Extensions, TOE, iONIC, iSCSI, iSER	٠
5 (*)	Communication systems: Software-directed power-aware interconnection networks Vassos Soteriou, Noel Eisley, Li-Shiuan Peh September 2005 Proceedings of the 2005 international conference on Compilers, architectures and synthesis for embedded systems CASES '05 Publisher: ACM Press	
	Full text available: pdf(895.11 KB) Additional Information: full citation, abstract, references, index terms	
	Interconnection networks have been deployed as the communication fabric in a wide range of parallel computer systems. With recent technological trends allowing growing quantities of chip resources and faster clock rates, there have been prevailing concerns of increasing power consumption being a major limiting factor in the design of parallel computer systems, from multiprocessor SoCs to multi-chip embedded systems and parallel servers. To tackle this, power-aware networks must become inherent c	
	Keywords : communication links, dynamic voltage, interconnection networks, networks on-a-chip (NoC), scaling, simulation, software-directed power reduction	
6	Architectural and performance evaluation of GigaNet and Myrinet interconnects on	
	clusters of small-scale SMP servers	
	Jenwei Hsieh, Tau Leng, Victor Mashayekhi, Reza Rooholamini November 2000 Proceedings of the 2000 ACM/IEEE conference on Supercomputing (CDROM)	
	Publisher IEEE Computer Society	

Additional Information: full citation, abstract, references, index terms

Full text available: pdf(82.49 KB)

GigaNet and Myrinet are two of the leading interconnects for clusters of commodity computer systems. Both provide memory-protected user-level network interface access, and deliver low-latency and high-bandwidth communication to applications. GigaNet is a connection-oriented interconnect based on a hardware implementation of Virtual Interface (VI) Architecture and Asynchronous Transfer Mode (ATM) technologies. Myrinet is a connection-less interconnect which leverages packet switching technol ...

Keywords: performance evaluation, high-speed interconnects, messagepassing interface, clusters of SMP servers

7	Optimizing 10-Gigabit Ethernet for Ne	etworks o	of Workstations,	Clusters,	and Grids: A
	Case Study				

Wu-chun Feng, Justin (Gus) Hurwitz, Harvey Newman, Sylvain Ravot, R. Les Cottrell, Olivier Martin, Fabrizio Coccetti, Cheng Jin, Xiaoliang (David) Wei, Steven Low November 2003 Proceedings of the 2003 ACM/IEEE conference on Supercomputing

Publisher: IEEE Computer Society

Full text available: pdf(209.19 KB) Additional Information: full citation, abstract

This paper presents a case study of the 10-Gigabit Ethernet (10GbE) adapter from Intel R . Specifically, with appropriate optimizations to the configurations of the 10GbE adapter and TCP, we demonstrate that the 10GbE adapter can perform well in local-area, storagearea, system-area, and wide-area networks. For local-area, storage-area, and systemarea networks in support of networks of workstations, network-attached storage, and clusters, respectively, we can achieve over 7-Gb/s end-to-end thro ...

Global signaling over lossy transmission lines

M. P. Flynn, J. J. Kang

May 2005 Proceedings of the 2005 IEEE/ACM International conference on Computer-aided design ICCAD '05

Publisher: IEEE Computer Society

Full text available: pdf(1.23 MB) Additional Information: full citation, abstract

We describe an interconnect scheme based on lossy transmission lines, compare this scheme with traditional bus based links, and present performance data. Unlike some other schemes there is no requirement for up-conversion, equalization, or special metal processing. In preliminary work, we have measured data rates of 14 Gbps (limited by test equipment) over a 7.2 mm interconnection, implemented in 0.18 /spl mu/m CMOS. For active links signaling over a single serial link, is more power efficient t....

Separated high-bandwidth and low-latency communication in the cluster interconnect [Clint

Hans Eberle, Nils Gura

November 2002 Proceedings of the 2002 ACM/IEEE conference on Supercomputing

Publisher: IEEE Computer Society Press

Full text available: pdf(235.04 KB) Additional Information: full citation, abstract, references, index terms

An interconnect for a high-performance cluster has to be optimized in respect to both high throughput and low latency. To avoid the tradeoff between throughput and latency, the cluster interconnect Clint has a segregated architecture that provides two physically separate transmission channels: A bulk channel optimized for high-bandwidth traffic and a quick channel optimized for low-latency traffic. Different scheduling strategies are applied. The bulk channel uses a scheduler that ...

10 Embedded systems à la carte

Peter Ryser, Michael Baxter

August 2002 Linux Journal, Volume 2002 Issue 100

Publisher: Specialized Systems Consultants, Inc.

Full text available: ntml(20:91 KB) Additional Information: full citation, abstract, index terms

Replacing hardware on the chip while dynamically loading the properLinux driver? No way!

11 A family of conservative codes with block delimiters for decoding without a phase-



locked loop

Yoram Ofek

February 1987 Proceedings of the 15th annual conference on Computer Science

Publisher: ACM Press

Full text available: pdf(433.39 KB) Additional Information: full citation, abstract, references, index terms

The family of conservative codes is a new scheme for encoding and decoding digital data for very high speed serial communication. These codes are characterized by having a constant number of transitions in each codeword and a known delimiting transition (rising or falling edge) at the end of each codeword. The conservative encoding scheme is primarily intended for binary data transmission in a single mode fiber optic network. Additional constraints imposed on the encoding are bal ...

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Authors

Wu-chun Feng

Los Alamos National Laboratory (LANL), NM Los Alamos National Laboratory (LANL), NM

Justin (Gus) Hurwitz Harvey Newman

California Institute of Technology (CalTech), Pasadena

Sylvain Ravot R. Les Cottrell California Institute of Technology (CalTech), Pasadena Stanford Linear Accelerator Center (SLAC), Menlo Park, CA

Olivier Martin

European Organization for Nuclear Research (CERN), Geneva, Switzerland

Fabrizio Coccetti Cheng Jin

Stanford Linear Accelerator Center (SLAC), Menlo Park, CA California Institute of Technology (CalTech), Pasadena Xiaoliang (David) Wei California Institute of Technology (CalTech), Pasadena

Steven Low

California Institute of Technology (CalTech), Pasadena

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↑ ABSTRACT

This paper presents a case study of the 10-Gigabit Ethernet (10GbE) adapter from Intel R. Specifically, with appropriate optimizations to the configurations of the 10GbE adapter and TCP, we demonstrate that the 10GbE adapter can perform well in local-area, storage-area, system-area, and wide-area networks. For local-area, storage-area, and system-area networks in support of networks of workstations, network-attached storage, and clusters, respectively, we can achieve over 7-Gb/s end-to-end throughput and 12-µs end-to-end latency between applications running on Linux-based PCs. For the wide-area network in support of grids, we broke the recently-set Internet2 Land Speed Record by 2.5 times by sustaining an end-to-end TCP/IP throughput of 2.38 Gb/s between Sunnyvale, California and Geneva, Switzerland (i.e., 10,037 kilometers) to move over a terabyte of data in less than an hour. Thus, the above results indicate that 10GbE may be a cost-effective solution across a multitude of computing environments.

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Catalin Meirosu, Piotr Golonka, Andreas Hirstius, Stefan Stancu, Bob Dobinson, Erik Radius, Antony Antony, Freek Dijkstra, Johan Blom, Cees de Laat, Native 10 Gigabit Ethernet experiments over long distances, Future Generation Computer Systems, v.21 n.4, p.457-468, April 2005

↑ Collaborative Colleagues:

Fabrizio Coccetti:

R. Les Cottrell Wu-chun Feng Justin (Gus)

Hurwitz Cheng Jin Steven Low Olivier Martin Harvey Newman Sylvain Ravot Xiaoliang (David)

Wei

R. Les Cottrell:

Antony Antony

Sylvain Ravot Xiaoliang (David) Wei

Fabrizio Coccetti Wu-chun Feng Justin (Gus) Hurwitz Cheng Jin Connie Logg Steven Low Olivier Martin Jiri Navratil

Harvey Newman

Wu-chun Feng:

Jeremy S. Archuleta Pavan Balaji

Adolfy Hoisie

Chung-Hsing

Michael Broxton Fabrizio Coccetti

Salvador Coll

R. Les Cottrell Adam Engelhart Mike Fisk Eitan

Frachtenberg Mark K. Gardner

Hsu Chung-hsing Hsu

Justin (Gus)

Hurwitz Cheng Jin Jane W.-S. Liu Steven Low

Olivier Martin

Harvey Newman

Richard Graham Dhabaleswar K. Panda

Fabrizio Petrini Ian Philp

Sylvain Ravot Sunil Thulasidasan

Peerapol '

Tinnakornsrisuphap Xiaoliang (David) Wei

Eric Weigle

Justin (Gus) Hurwitz:

Fabrizio Coccetti R. Les Cottrell Wu-chun Feng

> Cheng Jin Steven Low Olivier Martin Harvey Newman Sylvain Ravot Xiaoliang (David)

Wei

Cheng Jin:

Fabrizio Coccetti Harvey

R. Les Cottrell Newman Anwar Elwalid Sylvain Ravot Wu-chun Feng Danny Raz Yuval Shavitt Paul Francis Justin (Gus) Kang G. Shin Hurwitz Haining Wang Sugih Jamin Xiaoliang Yixin Jin (David) Wei Steven Low Indra Widjaja Olivier Martin Lixia Zhang Steven Low: Mung Chiang Olivier Martin Fabrizio Coccetti Harvey R. Les Cottrell Newman J. Doyle Sylvain Ravot Anwar Elwalid A. Tang Wu-chun Feng J. Wang Justin (Gus) Xiaoliang Hurwitz (David) Wei Cheng Jin Indra Widjaja David Lapsley L. Li Olivier Martin: Ron D. Appel Justin (Gus) Xiaoliang (David) Wei Marc Cavazza Hurwitz Nadine Zangge Fred Charles Cheng Jin Steven Low Fabrizio Coccetti R. Les Cottrell Xavier Marichal Wu-chun Feng Steven J. Mead Julien Frey Yoann Mescam Robin Gras Alok Nandi David Hernandez Harvey Patricia Newman Hernandez Jacques Nicolas Sylvain Ravot Harvey Arshad Ali Justin (Gus) Richard McClatchey Michael Thomas Newman: Hurwitz Ashiq Anjum Shawn McKee Xiaoliang (David) Tahir Azim Jang Uk In Atif Mehmood Wei Julian Bunn Saima Iqbal Dan Nae Ian Willers Julian James Cheng Jin Yang Xia Sylvain Ravot Búnn Faisal Khan Waqas ur Rehman Muhammad Adeel Richard **Iosif Legrand** S. Yousaf Shah Zafar Cavanaugh Frank van Conrad Steenberg Waqas ur Fabrizio Coccetti Lingen Conrad D. Steenberg Rehman R. Les Cottrell Steven Low Xun Su Frank van Lingen Wu-chun Feng Steven H. Low Rizwan Haider Olivier Martin Sylvain Ravot: Julian James Steven H. Low Bunn Olivier Martin Richard Shawn McKee Cavanaugh Dan Nae Fabrizio Coccetti Harvey R. Les Cottrell Newman Wu-chun Feng Conrad D. Justin (Gus) Steenberg Hurwitz Xun Su Cheng Jin Michael Thomas Iosif Legrand Xiaoliang

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Fabrizio Coccetti R. Les Cottrell Wu-chun Feng Justin (Gus)

Hurwitz Cheng Jin Steven Low Olivier Martin Harvey Newman Sylvain Ravot

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